REMARKS

Claims 1-4 and 13-21 are pending. Claims 1 and 20-21 have been amended. No new matter has been added.

Claims Rejections - 35 U.S.C. § 103

In the Action, claims 1-4 and 13-21 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Stallkamp (US 6,895,009) in view of Domon (US 2003/0014679).

In response, Applicant respectfully traverses these rejections, and Applicant respectfully asserts that the cited references, alone or in any combination, fail to disclose or suggest each and every limitation of the present claims.

In Fig. 1, Stallkamp discloses that AV device 108 receives a reference signal from reference signal line 102 and a clock signal from isochronous transport medium 104. In col. 3, lines 50-54, Stallkamp discloses that reference signal line 102 distributes a synchronization signal that is asynchronous to an isochronous clock signal distributed across isochronous network 104 by master 106.

In FIG. 2, Stallkamp discloses that AV device 108 comprises synchronizer 254 that receives a reference signal from reference signal line 102 via house reference signal line 255 (col. 5, lines 12-14) and timestamp information from I/O bus 250 (col. 5, lines 7-9). Also, in col. 5, lines 4-7, Stallkamp discloses that synchronizer 254 receives timestamp information from network controller 252 via side-band connection 253.

In FIG. 2 and col. 4, lines 65-67, Stallkamp discloses that network controller 252 receives isochronous network packets from isochronous transport medium 104 via isochronous signal line 257 and separates packet header information from the packet data. In col. 4, line 67 to col. 5, line 2, Stallkamp discloses that network controller 252 sends packet data to processor 210 via I/O bus 250. In col. 5, lines 3-8, Stallkamp discloses that network controller 252 recovers timestamp information from the received isochronous packet headers and sends the recovered timestamp information to synchronizer 254 via side-band connection 253.

Clearly, by the teachings of Stallkamp, synchronizer 254 does <u>not</u> directly receive packet data, as purported by the Action. Instead, according to Stallkamp, synchronizer 254 only receives a reference signal from reference signal line 102 via house reference signal line 255 and timestamp information from network controller 252 via side-band connection 253, and

synchronizer 254 does not directly communicate with isochronous transport medium 104, as clearly shown in FIG. 2.

Moreover, in FIG. 3, Stallkamp discloses that synchronizer 254 receives the reference signal from reference signal line 102 via house reference signal line 255 and timing information via isochronous signal line 357. As clearly shown in FIG. 3, synchronizer 254 comprises frame rate converter 304 that only receives local clock signal 302 via clock output 309 and only generates video clock signal 310. Frame rate converter does not directly receive any data signals from isochronous signal medium 104, and frame rate converter 304 does not convert image data in a manner as purported by the Action. Instead, as disclosed by Stallkamp in col. 5, frame rate converter 304 of synchronizer merely generates video clock signal 310 (col. 5, lines 61-63) to synchronize the operating frequency of AV device 108 with the operating frequency of AV device 110 (col. 5, lines 9-12), which is different than the subject matter of present claim 1.

Further, to the extent that Stallkamp suggests handling video data in col. 5, lines 58-67 and synchronizing video data in col. 1, lines 17-22, it is not clear by the teachings of Stallkamp of how data conversion is achieved. According to FIG. 3 of Stallkamp, frame rate converter 304 only receives a local clock signal from local clock 302 via clock output 309, and frame rate converter does not directly receive any data signals from isochronous signal medium 104 via isochronous signal line 357. Therefore, Stallkamp is not considered to explicitly teach each and every limitation of present independent claim 1, as purported by the Action.

In contrast to Stallkamp, present independent claim 1, as amended, recites the following limitations (***emphasis added***):

> a first node and a second node in which one of the first node and the second node on an IEEE1394 bus serves as a cycle master, the first node having a DV data processing unit configured to transmit first image data to the second node via the IEEE1394 bus at a transfer rate synchronized with a cycle start packet output from the cycle master, ***the second node having a data conversion unit configured to receive the first image data from the DV data processing unit of the first node via the IEEE1394 bus, convert the first image data to second image data by synchronizing the second image data generated by conversion of the first image data in the second node with an external reference signal, the second node to output the second image data via the data conversion unit,***
>
> an external synchronizing signal receiver for receiving the external reference signal provided on at least one of the first and second nodes, and
>
> a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external

reference signal received by the external synchronizing signal receiver, by carrying out feedback control of a clock source frequency of the cycle master using the external reference signal.

Support for these limitations of present independent claim 1 may be found throughout the present specification, for example, pars. 37-43.

The cited ancillary Domon reference fails to remedy the deficiencies of Stallkamp. For instance, Domon is merely relied on for purportedly teaching a digital video player 220 in Fig. 11 that decodes a digital video signal and outputs an analog video signal. To the extent that Domon suggests updating the timing parameters of slave nodes with a master timing signal, Domon fails to disclose or even suggest a second node having a data conversion unit configured to receive the first image data from the DV data processing unit of the first node via the IEEE1394 bus, convert the first image data to second image data by synchronizing the second image data generated by conversion of the first image data in the second node with an external reference signal, the second node to output the second image data via the data conversion unit, in a manner as recited in present independent claim 1.

Therefore, since the Stallkamp reference fails to disclose or even suggest each and every limitation of present claim 1, and since the ancillary Domon reference fails to remedy the deficiencies of Stallkamp, present independent claim 1 including any claims dependent thereon are considered to be in condition for allowance, and such allowance is respectively requested.

Claims 2-4 and 13-19 are dependent on independent claim 1 and therefore include all of limitations of independent claim 1 and additional limitations therein. As such, these claims are considered to be in condition for allowance for at least their respective dependence on present independent claim 1.

Present independent claims 20-21 have been amended similar to present claim 1 and are considered to be in condition for allowance for at least the same reasons as discussed above in reference to present independent claim 1, and such allowance is respectively requested.

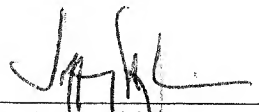
For at least the reasons discussed herein, present claims 1-4 and 13-21 are not anticipated or considered obvious over the cited references, alone or in any combination. Therefore, reconsideration of present claims 1-4 and 13-21 is respectfully requested with express withdrawal of the rejections under 35 U.S.C. § 103(a).

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-4 and 13-21 in the application are patentable. Accordingly, reconsideration and allowance of this application are earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

In the event that any fees are due with respect to this paper, please charge Deposit Account No. 01-2300, referencing Atty. Docket No. 033163-00762.

Respectfully submitted,



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